Design of DDIC data source driver signal digitizer to improve source signal level capture accuracy by calibrating out the parasitic capacitance of signal path using SPICE simulation

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ABSTRACT

Display driver integrated circuits (DDICs) drive 8-bit to12-bit level FPD (flat panel display) pixel signals in parallel across hundreds of channels. Each channel must drive these video pixel signals within strict levels and timing, but skew timing differences in signal delivery to the panel affect the overall video quality of the display. Typically, the primary causes of these slew and level errors are capacitance differences in each source driver or parasitic capacitance differences in the signal lines. If the source signal test circuit and the long signal delivery are not uniform, or if the loading capacitance values are not designed or manufactured to be less than 10% of source channel capacitance, the incorrect reading of the capacitance of the source driver will be missed sorting bad IC. Therefore, DDIC manufacturers must take the detection of source capacitance errors very seriously to maintain IC quality and ultimately display quality. In this paper, I present a SPICE (Simulation Program with Integrated Circuit Emphasis) simulation technique to measure signal line parasitic capacitance accurately and mathematically compensate it out from captured data to derive the correct DDIC source driver output load capacitance.

Keywords: SPICE, DDIC, FPD, OLED, TFT

1. INTRODUCTION

DDIC is an integrated circuit chip that controls the panel and display method of LCD panels and AMOLED panels. As panel displays frame rate, pixel size, and data transfer rates increase, requirements for driver ICs are also increasing.

In Figure 1, the OLED (Organic Light-Emitting Diode) DDIC is one of the main control components of the panel. Its main function is to control the light and color of the screen and transmit driving signals and data as electrical signals to the display panel to display text, photos, and other video information on the screen.

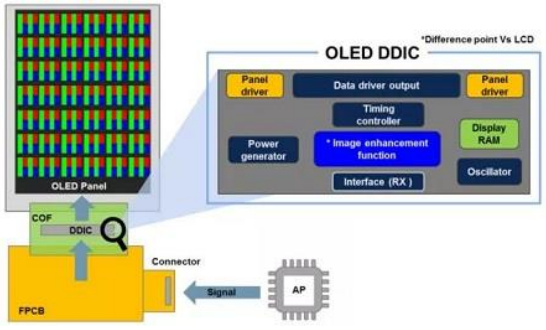

Figure 1. OLED DDIC connectional and block diagram

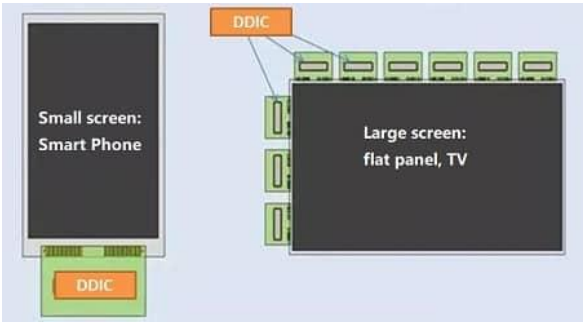

Figure 2. DDIC location

DDIC drives the display panel and transmits image data through electrical signals. In Figure 2, the location of the DDIC is differentiated depending on whether it is PMOLED or AMOLED. For PMOLEDs, the DDIC inputs current into both the horizontal and vertical ports of the panel. Upon current excitation, the pixel dots turn on, and the

brightness can be controlled by controlling the current level. In the case of AMOLED, each pixel corresponds to a TFT layer (Thin Film Transistor) and a data storage capacitor that controls the gradation of each pixel. Each pixel is made up of several subpixels representing the three primary RGB colors (R red, G green, and B blue).

The pixel voltage values (or on-state time duty cycle) of the TFT are transmitted one by one according to a certain time rhythm in a scanning manner.
Some of the ICs responsible for scanning are DDICs, some are responsible for horizontal, and some are responsible for vertical. As shown in Figure 3, the one responsible for horizontal work is called the Gate Driver IC (also called Row IC), and the one responsible for vertical work is called the Source Driver IC (also called Column IC).

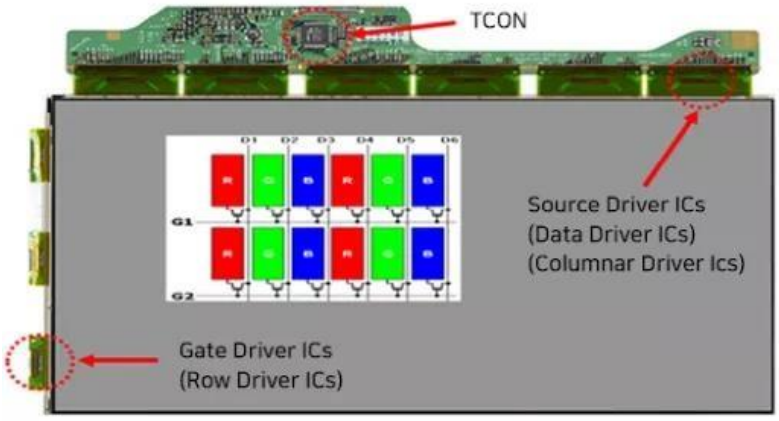

Figure 3. DDIC gate and source driver and TCON location on FPD

In order to obtain the best FPD image quality, the DDIC data signal source must be designed to drive the correct level and timing, and all channels must be designed symmetrically. However, the source signal meter channel of the ATE is about 0.6-1.0m away from the DDIC, and it is not easy to design a signal meter to accurately measure the signal due to the long signal transmission and the parasitic capacitance difference of each channel.

2. Measure DDIC Source driver with ATE digitizer channel

2.1. DDIC Source driver

A typical DDIC source driver block diagram is shown in Figure 4. However, in order to verify the V/I drive specifications of hundreds of DDIC source drivers in the IC, the source driver circuit is simplified as shown in Figure 5. This circuit is designed to have the same function and power drive performance by designing nearly identical series output resistor and load capacitor values for each channel. In particular, to verify the load capacitor values, which have much larger value variation than the series resistor, the test equipment with a very low pF accuracy capacitance measurement function on each channel must be designed.

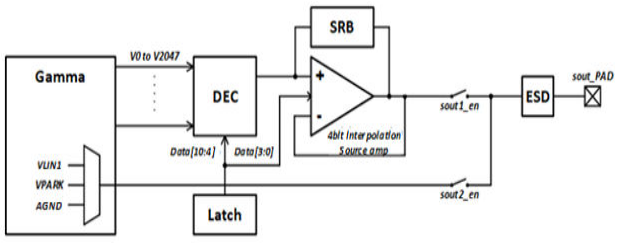

Figure 4. DDIC Source Driver block diagram

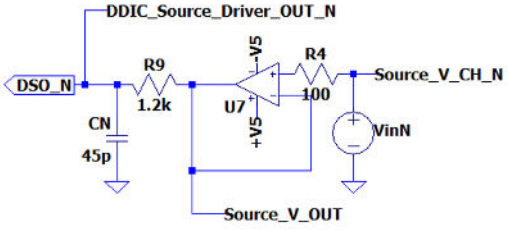

Figure 5. Simplyfied DDIC Source Driver SPICE model

2.2. DDIC Source driver signal Digitizer and loadboard Design

If the DDIC source channels are designed and fabricated uniformly and the signal paths to the capture device are ideally all the same, the voltage level of each source driver is expected to be the same simultaneously measuring by the digitizer or comparator. However, this relationship does not hold in real situations. First, if the load board design is asymmetrical with respect to the pattern length and width, the parasitic capacitance of each signal line pattern on the load board is not the same. Second, if the interconnections of each block of the instrument channel card (including all passive and active components, pogo blocks, and PCB signal patterns) are not symmetrical, the capacitance between channels will be unequal, making it difficult to accurately measure the source video signal level, and indeed the source-deriver channel capacitance.

As shown in Figure 6, the signal path of the DDIC source signal digitizer inside the channel card is composed of multiple layers of connections, relays, and other complex function blocks, which is much more complex than the load board path designed just with simple signal lines without passive or active components.

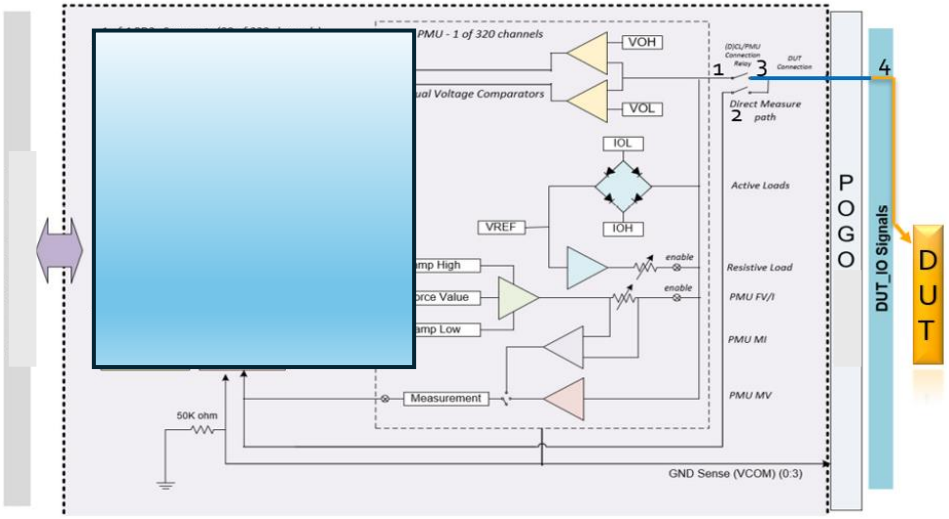

Fig 6. DDIC Source digitizer channel, POGO, Loadboard, and Socket (or Needle) connection Block Diagram

Therefore, these load board and digitizer instrument designs introduce unexpected line or path capacitances that are higher than the target load capacitance of the IC channel, making it impossible to accurately capture the source driver signal level or slew time, so the unquantized capacitance must be identified and the application values must be calibrated from the measured values.

2.2. DDIC Source driver and ATE Digitizer signal line integration modeling

ATE test systems are used to accurately and precisely measure the Cn of individual channels to classify devices as good or bad. These device tests provide information on the capacitance changes.

Each source channel is connected to the DDIC signal digitizer channel card located inside the test head through the following paths: 1. needle or socket, 2. transmission line on the load board, 3. pogo contact, 4. channel path inside the capture channel card, and 5. several functional blocks of the channel card for signal testing - as shown in Figure 7 - a. comparator for high-speed high-noise test, b. resistive load having multiple resistor arrays can select c. active load for loading +/- 2mA, d. DC meter for the prametric testing of the IC pin, and e. Digitizer to capture the video signal from the IC.

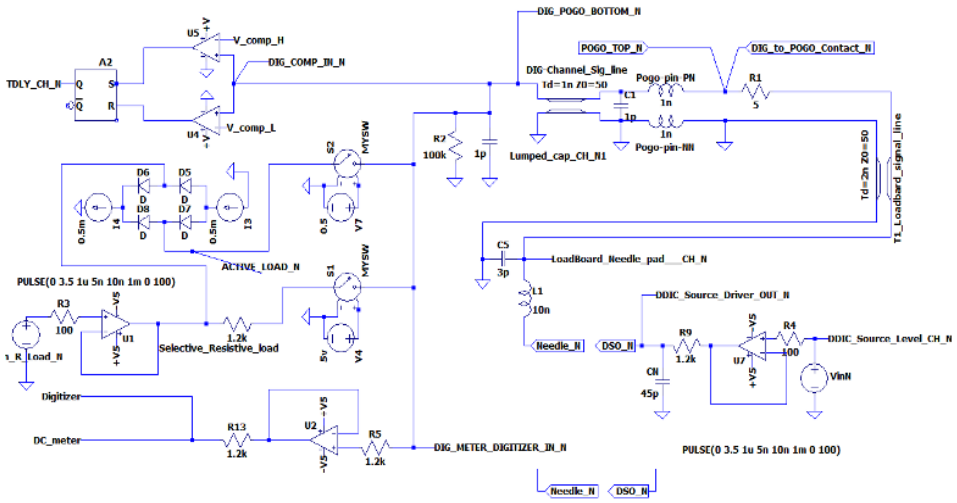

Fig 7. ATE DDIC digitizer channel card, Loadboard, and DDIC source channel signal line integreation model

3. How to extract the DDIC source channel capacitance (Cn) value correctly byremoving the chandigitizer channel and loadboard lump capacitance

To test the DDIC source channel video signal, connect the digitizer to the DUT (source signal driver pin) through the loadbpard signal path, drive a step signal to the digitizer, and then measure the signal RC time using the digitizer or a comparator as shown in Figure 6.

To accurately measure the DDIC source driver pin capacitance, first measure the lumped capacitance of the digitizer channel and the load board at the first test setup time, and apply this to the calibration value to extract the actual source driver capacitance value Cn from the signal measured from the DDIC source signal digitizer of the ATE system channel card.

Typically, a comparator is used in production testing to save test time, and a digitizer is used in evaluation testing.

3.1. DDIC Source driver capacitance calculation

If the DDIC source capacitance is 45pF designed as shown in Figure 8, you can measure the value by applying a 3.5V step pulse and check the response signal as shown in the blue line in the scopeshut. This is a simple RC signal of the source driver captured and simulated.

Since the source driver is designed with 45pF output capacitance in series with 1.2K channel resistor, we can determine the load capacitance Cn 45pF using the captured RC code using the following equations (1) and (2).

$$\mathbf{Vout(t) = Vsrc(t)\ [1\text{-}Exp\ \{-\ t/(Ro*Cn)\}]}\ \text{- (1)}$$

$$\mathbf{Cn = -t/[Ro*ln(1\text{-}Vout(t)/Vsrc(t))]}\ \text{- (2)}$$

Cn = -t/[1.2K*ln (1-Vout(t)/Vsrc(t))] = - 90.7ns / [1.2Kohm * ln(1-2.8V/3.5V)] = 45.41pF –(3)

The simulation result of Cn differs only by 0.91% from the design value of 45pf, which is much lower than the typical silicon wafer capacitance manufacturing error rate, as shown in Table 1. Therefore, this methodology and the circuit for the source channel loading capacitance test are verified.

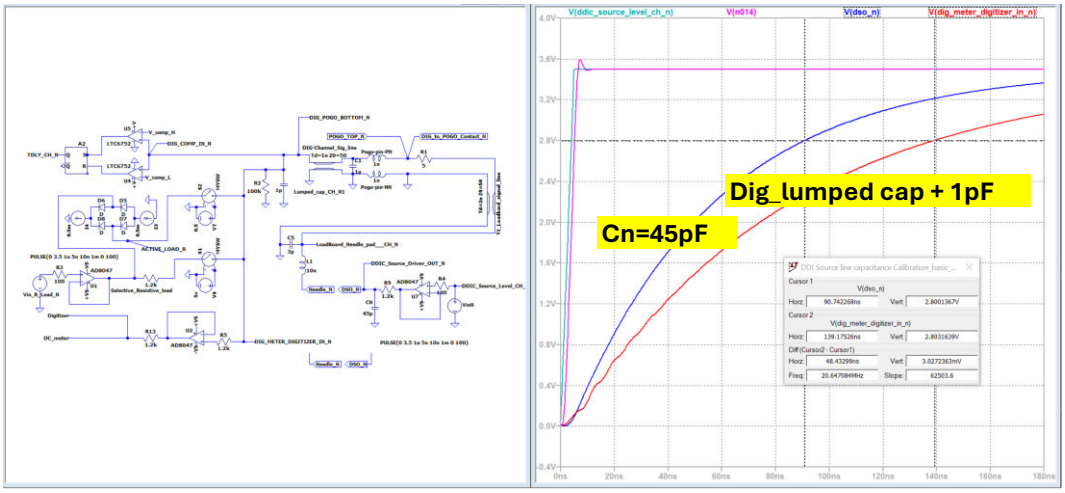

Fig 8. Response of Drive 3.5V step signal by a source chanel:BLUE, and Digitizer+Loadboard-RED

3.2. Lumped capacitance measure of ATE DDIC Source digitizer and Loadboard

To test the lumped capacitance of a digitizer channel, including the loadboard traces on the PCB, with a socket pin or a needle, first open the DUT and test the capacitance using the internal step pulse generator on the digitizer channel. Since the step signal generator has a small slew delay in the nanoseconds, the RC curve time must be compensated to obtain an accurate capacitance value from the formula.

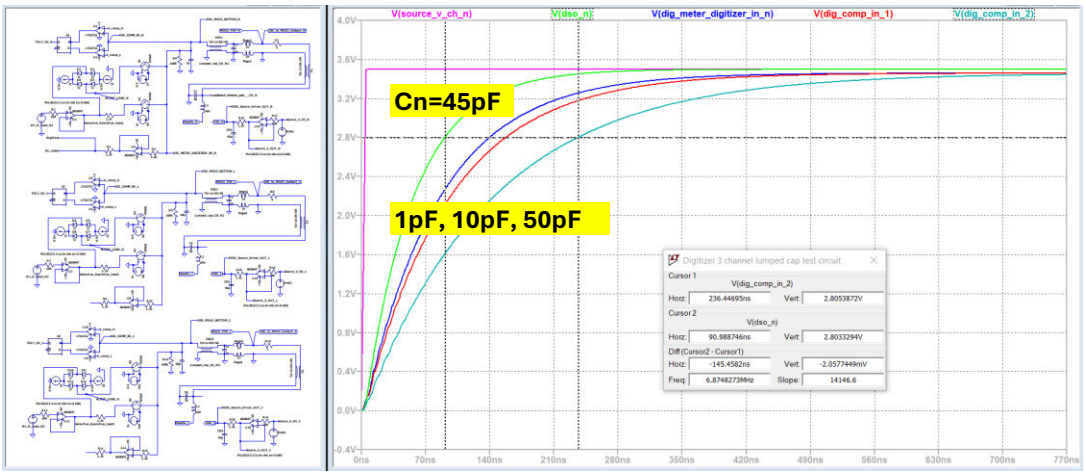

Fig 9. Response of 3.5V step signal with a 10pF, 10pF, and 50pF dig channel capacitors and Loadboard capacitance

Since the lumped capacitor change should be less than 40pF, simulated the step pulse response of the circuit while varying the digitizer channel capacitance from 1pF, 10pF, and up to 50pF and expected a linear charge time delay. Note that the step pulse generator slew delay is measured to be about 3ns, so to obtain an accurate RC charging time, need to recalculate the time by adding the slew delay.

To properly measure the DDIC source driver Cn value, the lumped capacitance values of hundreds of digitizer channels should be symmetrical and less than 1/10 of the source driver loading capacitance. However, each lumped capacitance of the digitizer channel lines connected to the load board are not the same, and the capacitance deviation between channels may be much higher than the source channel capacitance variation limit.

In order to check the capacitance of the channel card and load board, the dig_channel capacitance value was changed from 1 pF to 50 pF as shown in Fig. 9, and a simulation was performed to calculate each lumped capacitance using equations (3), (4), and (5).

$$C\_lumped\_1p\_open = 139ns / [1.185Kohm * \ln(1-2.8V/3.46V)] = 69.15pF \quad -(3)$$

$$C\_lumped\_10p\_open = 156ns / [1.185Kohm * \ln(1-2.8V/3.46V)] = 77.79pF \quad -(4)$$

$$C\_lumped\_50p\_open = 236ns / [1.185Kohm * \ln(1-2.8V/3.46V)] = 118.32pF \quad -(5)$$

The results of the capacitance reading error variations are within a +/- 0.27% error range as shown in Table 1, which is well below the design target capacitance variation limit of +/- 5%.

Digtizer+LB	Time	Ro	Vo	Vs	Total Cap (LB+DIG)	Design Target	Unit	Diff	SC Cn and LB+DIG Lumped Cap	Unit2
Cn(Reference)	9.07E-08	1200	2.8	3.50	45.41	45	pF	0.91%	45.41	pF
Dig_lumped_1p	1.39E-07	1186	2.8	3.46	69.15	69	pF	0.22%	69.15	pF
Dig_lumped_10p	1.56E-07	1186	2.8	3.46	77.79	78	pF	-0.27%	77.79	pF
Dig_lumped_50p	2.36E-07	1186	2.8	3.46	118.32	118	pF	0.27%	118.32	pF

Table 1. Lumped capacitance change and simulation traction linearity result

4. Extract the source driver channel capacitance from integrated signal line test result

To measure the DDIC source driver signal, first connect the DUT to the probe card needle or socket pins as shown in Figure 10, Source Driver and Capture Circuit. This circuit shows the connections for the "Needle_N" and "DSO_N" lines.

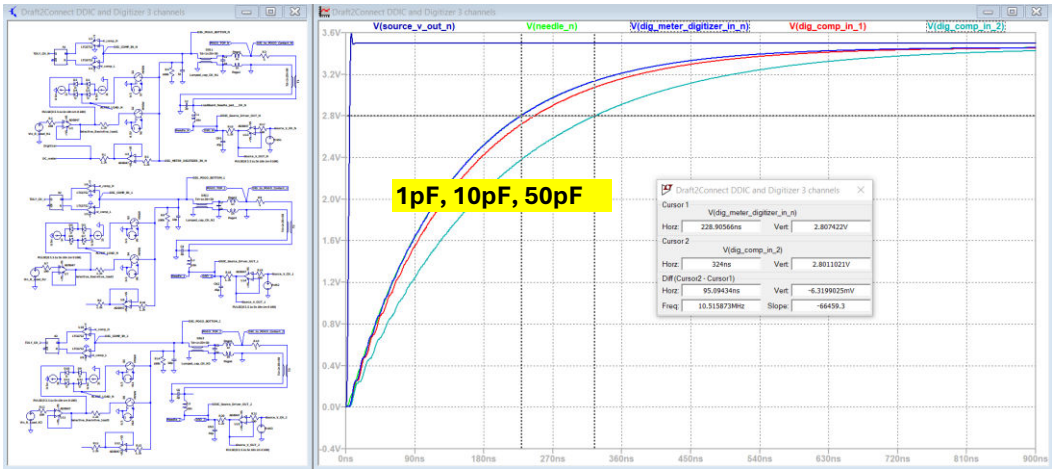

Fig 10. Response of DDIC Source 3.5V step signal with 10pF, 10pF, and 50pF Dıg-Channel + Loadboard capacitance

The results show that the merged signal line RC response time is longer than the open channel, as shown in Figure 10. This is because the total capacitance is increased by adding the lumped capacitors of the digitizer to DDIC source channel Cn. The captured total capacitance value is equal to the "Cn + lumped capacitance" value, as shown in Equations (6), (7), and (8).

CN1 = 114.91pF - 69.15pF = 45.76pF –(6)

CN2 =123.71pF - 77.79pF = 45.92pF –(7)

CN3 = 163.21pF - 118.32pF = 44.89pF –(8)

It also shows the circuit has capable of capturing the Source channel Cn capacitance variation less than 1% accuracy as shown in Table 2.

DDIC+Digtizer+LB	Time	Ro	Vo	Vs	Total Cap (DDIC+LB+ DIG)	Design Target	Unit	Diff	Source Channel Cap	Unit2
Dig_lumped_1p	2.29E-07	1186	2.8	3.46	114.91	114	pF	0.80%	45.76	pF
Dig_lumped_10p	2.46E-07	1186	2.8	3.46	123.71	123	pF	0.57%	45.91	pF
Dig_lumped_50p	3.24E-07	1186	2.8	3.46	163.21	163	pF	0.13%	44.90	pF

Table 2. Capture DDIC Source channel Capacitance Cn

4. CONCLUSIONS

As video frame rates increase, the DDIC source driver video signal level, rate, and timing accuracy have improved. Therefore, more accurate digitizer channels and low parasitic capacitance signal transmission line designs are essential for ATE systems. However, the parasitic capacitance of the test signal path is much higher than the source channel loading capacitance because it is consisted with the additional connectors and multiple functional circuits, this solution shows the how to calibrate out the unexpected parasitic capacitance on the test signal path . To accurately test ICs in ATE systems, the digitizer and signal transmission line capacitance must be designed and can be measured within 10% error. This paper presents a solution to measure parasitic capacitance within 2% error using RC curve time modeling of the source and digitizer channel signal integrity. In order to measure more accurately the source driver channel capacitance using this solution, it is necessary to compensate for the step pulse slew delay and accurately adjust the step pulse level attenuation affected by the long channel path or other active or passive components' loading in the test channel card and application path.

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