Cohu

DIAMOND$_x$ SERIES MP1$_x$

Optimized Solution for LVDS Port and DDR Memory Port Test

Highlights:

- Matching the interface structure and requirements of a DDR memory controller for simplified DUT boards
- Supporting built-in memory protocol support
- Same cycle match capability to support for data latency of up to 8 cycles

Features:

- Clock-forwarded and source synchronous LVDS capability for testing of high speed parallel communication interfaces such as MIPI D-Phy up to 1.1 Gbps
- Supports testing of 32 bit DDR and LPDDR DRAM memory port controllers up to 800 Mbps
- Built-in support for DDR protocol features such as CA bus and read training, write leveling, and DUT latency compensation
- Natively source synchronous for both transmit and receive
- 400 MV Vector Memory and 100 MV Fail/Data Capture Memory
- Per-pin levels and PMU

The MP1$_x$ instrument is designed to meet the high-volume testing challenges of integrated application-specific-standard-product (ASSP) devices driven by the Consumer, Mobility, Automotive and Internet of Things (IoT) markets.

DIAMOND$_X$ SERIES MP1$_X$

1. Basic Hardware Specifications

Channels per board	80
Ports 0 to 4:	1 differential clock pair puls 5 differential data pari, or 12 single ended
Ports 5 and 6	1 differential clock pair and 4 differential data paris, or 10 single ended

2. Basic Driver Specifications

Driver Levels, Per Channel	VHI, VLO, VTERM = (VHI+VLO)/2
Driver Levels Range	-0.3 V to 3 V
Driver Output Impedance	50 Ω
Driver Rise/Fall (2 V swing)	250 ps

3. Comparator

Comparator per channel	One Single Ended Per Channel, One Differential Per Channel Pair
Comparator Threshold	One Per Channel (Zero crossing differential)

4. Timing

Timing Accuracy Within a Port	
Driver Hi/Lo Transition EPA	+/-50 ps
Driver On to Hi/Lo Transition EPA	+/-150 ps
Comparator EPA	+/-50 ps
Intra-Port OTA	+/-100 ps
Timing Accuracy Between Ports	
Driver Hi/Lo Transition EPA	+/-100 ps
Driver On to Hi/Lo Transition EPA	+/-200 ps
Comparator EPA	+/-100 ps
Inter-Port OTA	+/-200 ps
Period Resolution	4.8828125 ps
Primary period range	0.9375 ns 1.875 ns
Decimation / Replication	1 to 128, powers of 2

5. Vector Pattern Generator

Maximum Data Rate	1066 MT/s (ports 0-3), 800 MT/s (ports 0-7)
Vector Memory	409 M vectors
Single Pass Match Range	8 UI
Pattern Opcodes	Repeat (mod 8), Loop, Jump, Flag, Stop, Keepalive, Match Align
Keepalive Pattern	32-2040 Vectors
Fail/Data Capture memory	215 M Vectors
PPMU Range	-1 V to +3.5 V, 4 µA to 40 mA

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