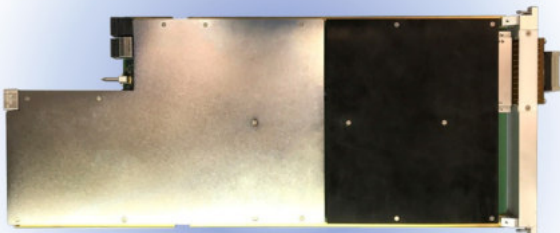


DIAMOND_x SERIES HSI_{1x}



Scalable, Cost-Efficient Solution for High Performance SerDes Test

Highlights:

- Physical layer testing with built in PRBS BERT TX/RX
- BIST/DFT testing using high bandwidth drive/compare memory
- Protocol level mixed-signal testing using deep send pattern memory

Features:

- Test of high speed serial ports with data rates up to 12.8 Gbps, such as HDMI, MIPI, JESD204, PCIeexpress, SATA, EPD, Vby1 and USB3
- 32 differential TX channels
- 24 differential RX channels
- Hardware clock data recovery per lane with flexible BERT sync
- Deep source memory
- Flexible loopback modes including closed loop BERT
- Calibrated jitter injection on all lanes
- Flexible pre-emphasis and equalization

The HSI_{1x} is optimized for testing clock-embedded and clock-forwarded serial interface commonly found in modern mobile, consumer, industrial and automotive electronics. These ports connect modems, cameras, displays, storage and applications processors to enable high bandwidth, low power consumption, and low EMI.

DIAMOND_x SERIES HSI1_x

1. Data Rate

Data rate range	400 Mbps to 12.8 Gpbs
Frequency resolution	1 KHz

2. Transmitter

Number of differential TX channels	32
AC output differential impedance	100 Ω
Differential voltage swing	40 mV to 950 mV
Pre-emphasis range	+/-300 mV (Typical)
Jitter Frequency range	0.1 KHz to 20 MHz
Max injected deterministic jitter, peak-peak	1.4 ns
Maximum RMS Random jitter injection	0.1 UI

3. Receivers

Number of differential RX channels	24
AC input differential impedance	100 Ω
Input differential voltage range	25 mV to 1.4 V
Input single ended range	360 mV to 1070 mV
Programmable comparator threshold voltage	+/-0.5 V
Extracted clock domains	2
Equalization gain	1 to 2.4

4. Pattern Specifications

Built in patterns	K28.5, PRBS 5, 7, 9 11, 13, 15, 21, 23 ,31, and invert, toggle, all ones, all zeros
Pattern segment size	512 bits – 64 Kbits
Total memory space for TX	8 Gb
Total memory space for RX	2 Mb
Sequence control	Loop infinite, Loop on count, Play to end
Maximum loop count per sequencer slot	$2^{*}16 - 1$
Triggering	External or internal

All specifications are subject to change without notice.

