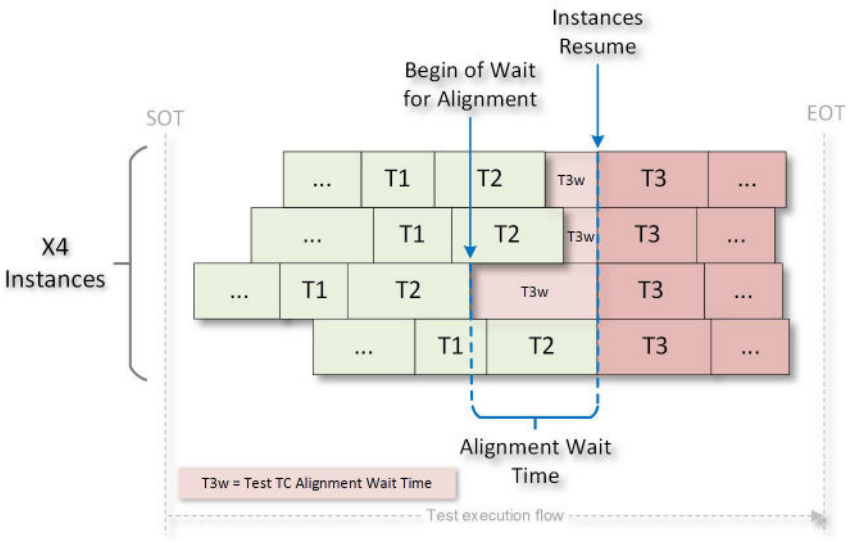
Unison Instancing eLearning

Introduction to Multi-Instances of Unison (MIU)




Automotive

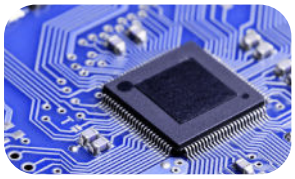

Mobility


IoT/IoV & Optoelectronics


Flat Panel Dislay


Industrial & Medical


Consumer


MCU

Course Description

This course serves as an introduction for users looking to understand the basics of Unison Software Instancing; sometimes referred to as Multi-Instances of Unison (MIU). Instancing enables parallel testing, optimizes resource utilization, and significantly enhances multi-site efficiency. On completion of this course, the student will be able to recognize the benefits of using Instancing, describe how Instancing improves Parallel Test Efficiency (PTE), identify programming implications, and state useful changes to their AdapterBoard design and Test System configuration when using Instancing. This is accomplished by multimedia presentations and knowledge checks.

Course Outline

- Instancing Overview
- Instancing Theory
- Instance Maps and Loading Programs
- Instance Alignment Anchors
- Hardware and AdapterBoard Design

Course Length

- Self-paced – 2-4 hours typical depending on skill level

Prerequisites

- Six months test program experience
- Successful complete of Unison Applications Programming ILT Class

Recommended

- C or C++ programming
- Familiarity with Linux Operating System
- English - written and spoken

- **Potentially Improves Parallel Test Efficiency (PTE)**
- **Facilitates execution of multiple Instances of Unison**
- **Supported on DxV and Diamond$_x$ Test Systems**
- **Runs on Unison U2023 (and beyond)**
- **Supports Instance debugging**

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Course Modules

1 - Instancing Overview

On completion of this lesson the student will be able to:

- Describe the purpose and elements of Unison Instancing
- Recognize how Instancing can lead to improved Parallel Test Efficiency (PTE)
- Summarize common Instancing Terms and Concepts

2 - Instancing Theory

On completion of this lesson the student will be able to:

- Recognize Test System configuration differences between using and not using Instancing
- Describe the mathematical basis for Parallel Test Efficiency (PTE) and how Instancing can improve it
- Summarize the factors that help to achieve Optimal Instancing Performance

3 - Instance Maps and Loading Programs

On completion of this lesson the student will be able to:

- Recognize the areas of the Unison PackageTool used to define and edit an Instance Map
- Identify the structure of an ASCII Instance map in a UNA file
- Summarize the Test Program loading features used to support Instancing within Developer

4 - Instance Alignment Anchors

On completion of this lesson the student will be able to:

- Describe Instancing asynchronous test program flow behavior
- Identify how Instance Alignment Anchors can lessen the impact of shared System Resources
- Recognize how to set Test Group (Flow Node) and API-based Alignment Anchors
- Summarize key concepts supporting Instance Alignment Anchors
- Summarize the UTL Instance Class APIs

5 - Hardware and AdapterBoard Design

On completion of this lesson the student will be able to:

- List the instrument and test system hardware that supports Instancing
- Recognize the role instrument segmentation plays in support of Instancing
- Summarize Instancing implications related to SDU CBITS, SDU utility power and Digital Triggering
- Identify Instancing AdapterBoard design and system configuration principles

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Who Should Attend

- Test program development and support engineers

Related Classes

- Unison Applications Programming
- Introduction to Unison eLearning

Course Viewing Requirements

To view the course, you must have:

- Browser supporting HTML5
- Audio-listening capabilities (such as a headset or speakers)
- Connection speed of at least 1.2 mbps

Course Cost

- Access is free of charge for all Cohu Semiconductor Tester Customers

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